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Modeling of the thermal effects of heat generating devices in close proximity on vertically oriented printed circuit boards for thermal management applications

Jared Harvest [a], Amy S. Fleischer [b,*], Randy D. Weinstein [c]

[a] *Department of Mechanical Engineering, Villanova University, Villanova, PA 19085, USA*
[b] *Department of Mechanical Engineering, Center for Advanced Communications, Villanova University, Villanova, PA 19085, USA*
[c] *Department of Chemical Engineering, Center for Advanced Communications, Villanova University, Villanova, PA 19085, USA*

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Abstract

The localized thermal interactions between adjacent devices on vertically orientated circuit boards in natural convection are predicted using experimentally validated computational fluid dynamics models. The effects of power density, device proximity, device geometry, circuit board material, board packing density and board separation distance on the steady state operating temperatures are investigated and incorporated into mathematical models which can be used to design packages which minimize thermal interactions. The separation distance beyond which the devices do not thermally influence each other is identified and the influence of various parameters on this distance is studied. The parametric study is designed using Design of Experiments methodology and therefore can be used to interpret the interaction between independent parameters. The developed models and methodology can easily and quickly be applied to other packaging situations to help minimize negative thermal interactions as one consideration in board layout design.

Keywords: Thermal management of electronics; Electronics cooling; Natural convection; Cooling of printed circuit boards; Vertical printed circuit boards; Device cooling computational

1. Introduction

The design of heavily populated circuit boards, with many heat generating devices in close proximity, presents a unique thermal challenge. With closely packed devices, some high power density devices may exert a heating influence on nearby devices, thus raising the neighboring device's operating temperature above recommended limits. The effects of board conduction, thermal wake interactions, and thermal plumes must be thoroughly investigated in a simple and accurate manner to allow designers to place devices on a closely packed circuit board without creating thermal interactions. The study presented here explores these thermal interactions and develops a methodology to quickly and accurately predict the influence of design parameters on steady state operating temperatures of devices on circuit boards in close proximity.

Several previous studies have been carried out to investigate the thermal influence of neighboring devices in natural convection. However, these primarily focus on uniformly spaced vertical arrays of uniformly heated elements, not on neighboring devices with unequal power dissipation or with varying separation distances. Although these studies are excellent foundations for our current work, the previous investigations were not designed to minimize thermal interaction.

In a classic study, Ortega and Moffat [1] present experimental results for free convection from a vertical plane with 80 protruding, geometrically-identical, identically-heated elements with a shrouding wall creating a channel flow situation. The development of the boundary layer over rows of succes-

* Corresponding author.
E-mail addresses: jared.harvest@villanova.edu (J. Harvest), amy.fleischer@villanova.edu (A.S. Fleischer), randy.weinstein@villanova.edu (R.D. Weinstein).

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Nomenclature

g	gravity	$m^2\,s^{-1}$	
Gr	Grashof number		
L	characteristic length	m	
P	power	W	
R	resistance	Ω	
T	temperature	K	
V	voltage	V	
β	thermal expansion coefficient	K^{-1}	
ν	kinematic viscosity	$m^2\,s^{-1}$	

sive elements and its influence on the operating temperature of the elements is presented. The natural convection flow over the protruding elements creates a turbulent wake resulting in heat transfer 40–50% higher than for the corresponding laminar situation while the element temperature increases with increasing row number until leveling off at a value 17% higher than the first row temperature. Moffat and Ortega [2] extend this study to show that although the actual physical situation is free convection, when the shrouding wall is in place at close distances, the resulting heat transfer agrees within 5% of accepted forced convection correlations.

Fujii et al. [3] model the natural convection from an array of five vertical parallel plates, each with a uniform 8×8 array of identically heated elements. The heat transfer results are again well-correlated according to a forced convection relationship despite the free convection situation. Park [4] studies the effect of channel spacing on free convection from two vertical parallel plates each with four identical protruding heat sources mounted in a constant temperature enclosure. The relatively high velocity flow which rises up along the heated plate is found to directly affect the heat transfer of the upper sources. The effects of thermal wakes have been characterized and studied for flush-mounted and protruding surfaces on horizontal and vertical surfaces [5–10]. Newport et al. [5] provides interferometry and particle image velocimetry images of two vertical printed circuit boards with protruding rib elements. The results show that the buoyant plume from on heated rib flows over the others, creating enhanced convection.

The effect of circuit board materials on the in-plane board conduction for a single heat source on a horizontal board is examined by Lohan et al. [11]. Circuit board material is found to have a significant effect on the operating temperature and in certain cases up to 75% of the heat dissipation from the heat source is found to occur through circuit board conduction. Guenin et al. [12] also show 74–89% of power dissipation for small outline integrated circuit packages (SOIC) occurring by conduction into the board itself. Several studies [5,13–15] have shown that the circuit board conductivity has a strong influence on the device operating temperature for arrays and single devices on horizontal and vertical boards.

The common result in these studies [1–15] is that thermal boundary layer from one heated element will influence another, often significantly, when in close proximity. Hence the device temperature and heat transfer from one element is affected by its neighbors. These studies provide valuable insight into the interaction of adjacent identical heated elements through board conduction and thermal plumes and into natural convection from discrete elements mounted in identical arrays on vertical printed circuit boards. However, none of these studies directly investigate the device spacing within which this neighbor interaction occurs. Nor do these studies examine the important packaging design parameters (power density, board material, number of boards, spacing between boards, and device separation) which may affect this spacing for protruding discrete sources on vertical boards in natural convection.

The purpose of this work is to investigate the device spacing within which devices thermally influence each other for two independently powered protruding devices located side-by-side on a vertical circuit board. The influence of significant design parameters on this distance and on the device operating temperatures will be quantified. When located within this spacing, the device operating temperature will be strongly affected by its neighbor, leading to possible overheat and reliability concerns. Natural convection and board conduction will be the primary methods of power dissipation with some dissipation also occurring by radiation. The side-by-side orientation (same horizontal plane) of devices is common on printed circuit boards and to some extent reduces the effects of thermal wakes. This study will investigate the dominant influences on thermal interaction in this arrangement. The study will be modeled numerically and the model will be validated against the experimental work of Fleischer and Weinstein et al. [16,17] which consists of experimental studies on device proximity effects on horizontal and vertical boards in free and forced convection. The use of numerical models in the current study allows the analysis of the effects of more parameters which include device geometry, circuit board fabrication, power ratio between devices, number of boards and spacing between boards.

2. Numerical analysis

The commercially packaged computational fluid dynamics software, IcePak 4.1 is used for the numerical modeling. IcePak is object-based modeling software with pre-defined objects specific to the electronics industry, once the model is created, IcePak uses Fluent 5.6, to numerically solve the conservation of momentum and energy equations. The model consists of the active computational regime, called the “cabinet”, the printed circuit boards and devices. Each board contains two devices.

The cabinet forms the extent of the computational domain and is modeled as an air-filled rectangular space with the top and bottom of the space completely open to allow ambient air flow freely in and out. The four side walls are impenetrable. This replicated a vented enclosure with vents on the top and bottom to encourage natural convection circulation. The extent of

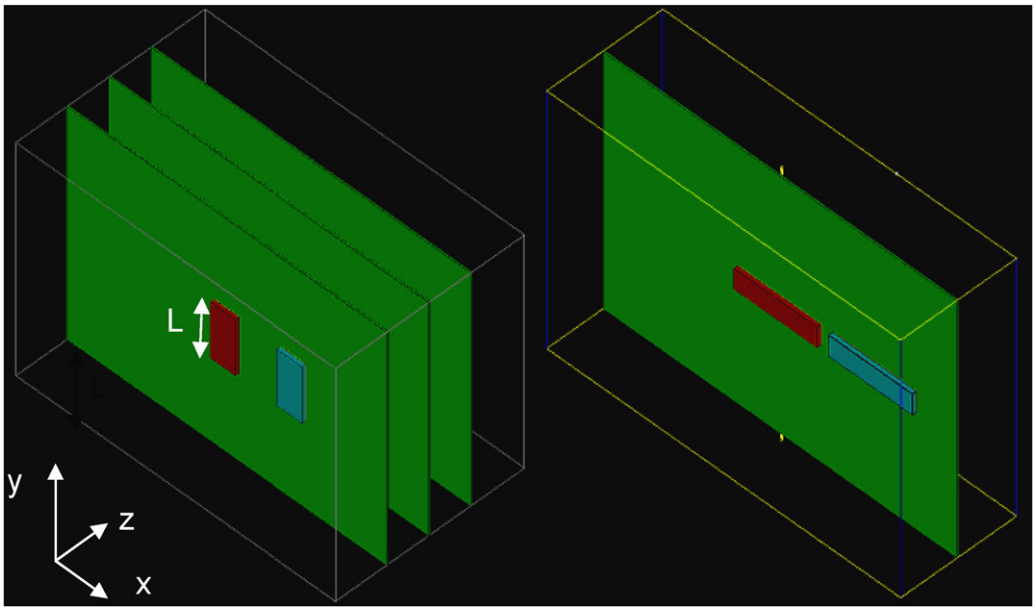


Fig. 1. Models illustrating tall rectangle geometry (left) and long rectangle geometry (right).

the regime is $305 \times 222 \times 150.0$ mm^3, large enough to contain several vertically orientated circuit boards. A sensitivity analysis was done on the size of the domain and on the number of free openings into the domain. The results were insensitive to the domain size and number of side openings and thus the smallest and simplest effective domain size was selected to minimize computational effort.

The circuit boards are modeled as FR4 boards $305 \times 222 \times 1.27$ mm^3. The bottom left corner of the board has the (x, y) coordinates of $(0, 0)$. All coordinates are presented in mm. The circuit board properties vary depending on the type of board selected as will be discussed below. The devices are modeled generically as two geometrically-identical blocks 3.2 mm thick and of varying dimensions (discussed below). The first device is located toward the center of the board such that its bottom left corner dimension is $(126.1, 98.8)$. The second powered device is located in close proximity to the first device such that the dimensions of its bottom left corner are $(x, 98.8)$ where $x =$ 178.9, 182.9, 187.9, 192.9, 202.9 or 212.9 mm. An example of this arrangement can be seen in Fig. 1. The devices are modeled so that they match the validating experimental arrangement [16, 17] in which the devices were attached to the board using a thermally conductive interface material ($k = 1.6$ W m^{-1} K^{-1}), assuring good contact between the source and the board, and thus serving as an upper bounding condition for various real applications in which the devices may attach to the board in a variety of different ways including ball grid arrays and leaded packages.

The boundary conditions are defined as laminar natural convection and radiation for all surfaces with an initial temperature of the air-filled domain set to 25 °C. Radiation is enabled in the computational model and view factors between all objects are computed. The computational domain consists of 86 436 nodes. To ensure mesh independence, the results were compared to a model with 323 431 nodes and the results were found to vary less than 1.2%.

The parametric study is designed using Design of Experiments (DOE) methodology to interpret the interaction between parameters. The DOE methodology allows parameter interactions to be explored when varying one parameter may cause a second parameter to affect the problem differently and offers advantages in interpretation over the traditional one-factor-at-a-time approach [18]. DOE mapping also allows the interaction between parameters to be explored with fewer trials than the traditional methodology. A full factorial DOE matrix is the most complete set of trials and analyzes the individual effect of each parameter (A, B, C) as well as the effects of parameter interaction (AB, AC, BC, ABC) [18]. For this analysis, the five parameters were organized into a matrix of 27 different analysis cases using a five factor face-centered central composite DOE (FCCCD) model to determine the ideal numerical tests to run for the five parameters of interest: board packing density, board conductivity, device geometry, power density, and board separation distance. An FCCCD model allows a full analysis of the influence of each parameter when each parameter is assigned a high and low value and a third value that varies linearly with the other two. Each parameter is assigned a number of -1, 0 or 1 starting with the lowest value and progressing to the highest value. That parameter is then set for each analysis run by the defined values in the matrix of experiments. The parameters are set as described below:

- Board conductivity is the thermal conductivity of the printed circuit board and is varied such that in-plane conductivity varies linearly from -1 to 1 according to:
  - -1: plain FR4 board ($k = 0.57$ W m^{-1} K^{-1} in-plane, 0.36 W m^{-1} K^{-1} through-plane). This is the limiting condition for the worst case board conduction results

and closely resembles a sparsely packed board with few traces.
  - 1: FR4 board with one ounce of copper cladding on the top surface to simulate a limiting condition for best case board conduction results with a circuit board with densely packed traces on the top layer. For the copper layer, thickness = 0.0003556 m, $k = 386\ \mathrm{W\,m^{-1}\,K^{-1}}$. For the FR4 layer, all properties remain as in the −1 case.
  - 0: FR4 board with a layer of cladding on the top surface to create a situation such that the conductivity takes the mean value of copper and FR4, so that for proper use of the DOE method a linear variation in conductivity is maintained from the −1 to 0 to 1 case, where the −1 and 1 cases are the limiting conditions. The cladding layer has the properties: thickness = 0.0003556 m, $k = 193\ \mathrm{W\,m^{-1}\,K^{-1}}$. For the FR4 layer, all properties remain as in the −1 case.
- Device geometry is the physical width and length of the devices. The length of the device in the vertical direction changes linearly while the total area in contact with the circuit board is maintained constant at $1285 \pm 4\ \mathrm{mm^2}$ so the total heat flux, $\mathrm{W\,m^{-2}}$, remains constant. The length and width vary in the x and y direction as:
  - −1 = 17.9 × 72 mm (tall rectangle).
  - 0 = 35.8 × 35.8 mm (square).
  - 1 = 53.6 × 24 mm (long rectangle).
- Power density is the ratio in applied power from one device to the other. The device that varies in location remains constant in power at 2.5 W while the device that maintains constant in location (126.1, 98.8) varies in power and takes the values 5.0 W, 7.5 W and 10 W. Thus the power ratio varies as:
  - −1 = 2 : 1.
  - 0 = 3 : 1.
  - 1 = 4 : 1.
- Board density is the number of identical circuit boards and varies as:
  - −1 = 1 board.
  - 0 = 2 boards.
  - 1 = 3 boards.
- Board separation is the distance between adjacent identical circuit boards and varies as:
  - −1 = 10 mm.
  - 0 = 25 mm.
  - 1 = 40 mm.

The DOE designed matrix of test runs is designed to optimize the interaction between the five parameters and to yield data on the operating temperature of each device as a function of device spacing and each independent parameter. Data from the computational model on power dissipation through conduction into the board, power dissipation through convection off the face of the device, radiation off the devices, heat transfer coefficient on the device face, velocity over the device and extent of the thermal footprint is also available from each test run. The DOE matrix analysis yields a regression model for the final result.

The Grashof number (Gr) is used to determine whether the natural convection has a laminar or turbulent flow regime. Eq. (1) is used to determine the Grashof number. The volumetric thermal expansion coefficient (β) is calculated for air at ambient temperature using the ideal gas approximation ($1/T$). The characteristic length (L) is in the direction of gravity and therefore is the device's height. The difference in temperature is the average steady-state temperature of the device minus the ambient. In all cases the calculation of the Grashof numbers places the model in the laminar regime.

$$Gr = \frac{g\beta(T_{\mathrm{device}} - T_{\mathrm{ambient}})L^3}{\nu^2} \tag{1}$$

3. Model validation

For validation, the numerical models are compared to experimental measurements for two heat sources independently powered on a vertically orientated FR4 board with natural convection. A complete description of the experimental equipment and procedure can be found in [16], while only the pertinent details are repeated here for completeness. Two aluminum plate heat sources $50.8 \times 25.4 \times 3.2\ \mathrm{mm^3}$ are mounted on a $305 \times 222 \times 1.3\ \mathrm{mm^3}$ FR4 board. A Kapton heater under each aluminum plate is independently controlled using a variable power supply. A type-T thermocouple with an outer diameter of 0.8 mm located in the center of each plate measures source temperature, and six other type-T thermocouples measure room temperature at various locations surrounding the board. A series of experiments is conducted with the two heat sources located at various positions on the board. The voltage to each heater is adjusted as necessary to allow one heat source to reach 60 °C above ambient and the other to reach 100 °C above ambient. The data collected is reduced to determine the power dissipated by each heat source at the target temperature versus the distance between the two heat sources.

The total power supplied to the heat source (P_{supplied}) is obtained using the voltage measurements across the heater (V_{heater}), and the known resistance of the heater (R_{heater}) under load conditions.

$$P_{\mathrm{supplied}} = V_{\mathrm{heater}}^2 / R_{\mathrm{heater}} \tag{2}$$

This power represents the total amount dissipated by the heat source through convection and radiation to the surroundings and through conduction into the board itself. A small amount of heat is dissipated through heat losses along the thermocouples which act as infinite fins. Heat losses due to this fin effect are calculated considering the metallic thermocouple wire to act as a fin along its length. Fin calculations show this amount to be less than 1.5% of the total power, which is then reduced by this value. Repeatability of the results is verified by multiple runs. The results are found to be repeatable within 5% in total power dissipation for each specified location.

The power dissipation from the numerical model for two heat sources maintained at 60 °C and 100 °C above ambient in side by side orientation on a vertical circuit board was compared to [16] and the power dissipations agreed within 6%, validating the model. The data comparison can be seen in Fig. 2.

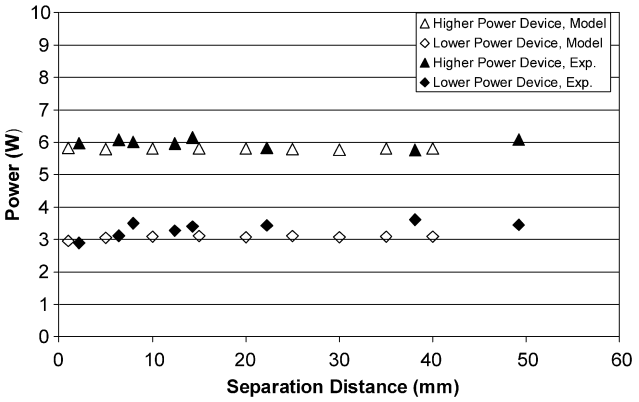


Fig. 2. Experimental validation of model.

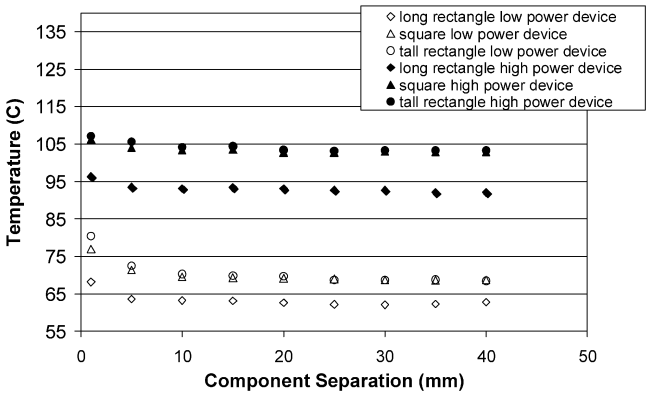


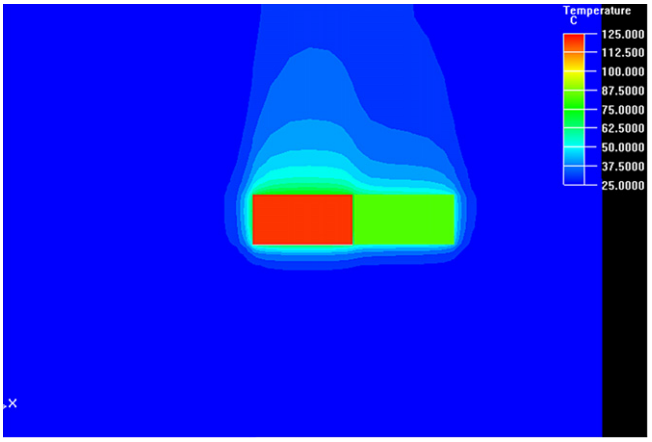
Fig. 3. Device operating temperature as a function of device geometry for a single FR4 board, 2 : 1 power ratio.

4. Results and discussion

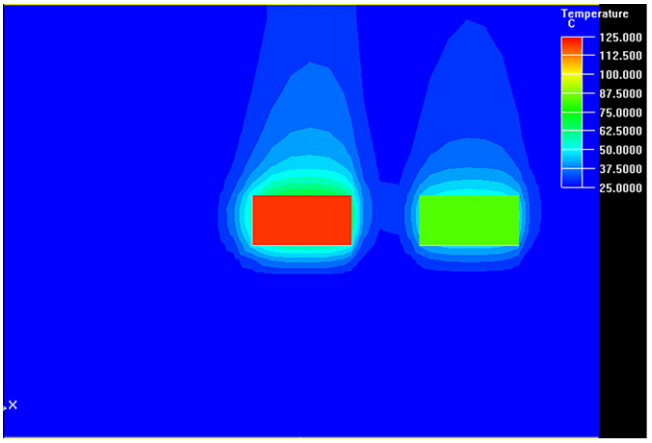
The purpose of this work is to investigate the device spacing within which devices thermally influence each other for two independently powered protruding devices located side by side on a vertical circuit board. The effects of device geometry, circuit board fabrication, power ratio between devices, number of boards and spacing between boards on device operating temperature are investigated. The methods developed here will allow designers to quickly explore design parameters and identify those with the most influence on thermal interactions so that these interactions can be minimized or eliminated in the final product.

The results show that when two powered devices are within a certain threshold spacing, referred to here as plateau spacing, the higher power device thermally influences the lower power device by increasing the operating temperature of the lower power device. At device spacing exceeding the plateau spacing, each device reaches an operating temperature that is independent of spacing. This operating temperature is referred to as the plateau temperature and remains constant as the spacing between devices continues to increase.

An example of this interaction can be seen in Fig. 3. Fig. 3 depicts the device operating temperature for two devices powered at 2.5 W and 5.0 W on a single FR4 circuit board. When the separation between the two devices is more than 10 mm, the device operating temperature remains constant at the plateau temperature. When the devices are spaced less than 10 mm apart, the operating temperature of the lower power device increases. As the separation distance decreases to as little as 1 mm, the peak operating temperature of the low power device is found to increase almost 9% from the plateau temperature (62.5 °C to 68.2 °C) for the long rectangles and as much as 16% (68.8 °C to 80.4 °C) for the tall rectangles. This increase of 12 °C can have a significant affect on device reliability and lifespan. A smaller increase in operating temperature is seen in the high power device. The peak operating temperature increases 4.5% (92.1 °C to 96.3 °C) for the long rectangles and 3.7% (103.3 °C to 107.1 °C) for the tall rectangles. Even these relatively small temperature rises can have detrimental effects on the lifetime of devices and need to be minimized or eliminated in many packages.



(a)



(b)

Fig. 4. Sample thermal footprints of devices at (a) 1 mm spacing and (b) 35 mm spacing.

For this natural convection situation, the spacing within which the devices thermally influence each other corresponds most closely to the conductive thermal footprint that the devices create on the printed circuit board. When the thermal footprints overlap as shown in Fig. 4(a) there are significant neighbor effects, and when the thermal footprints do not overlap as shown in Fig. 4(b), the neighbor interaction is limited.

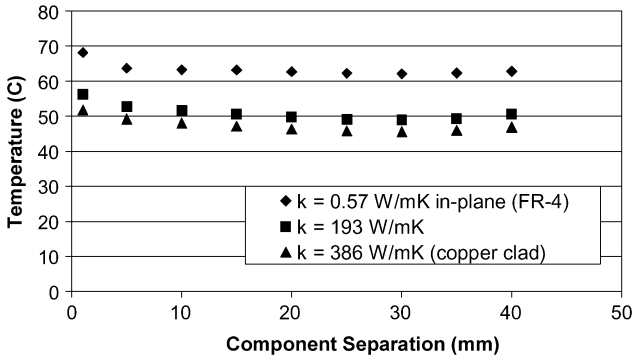


Fig. 5. Device operating temperature as a function of circuit board design for a single board, 2 : 1 power ratio, long rectangle device.

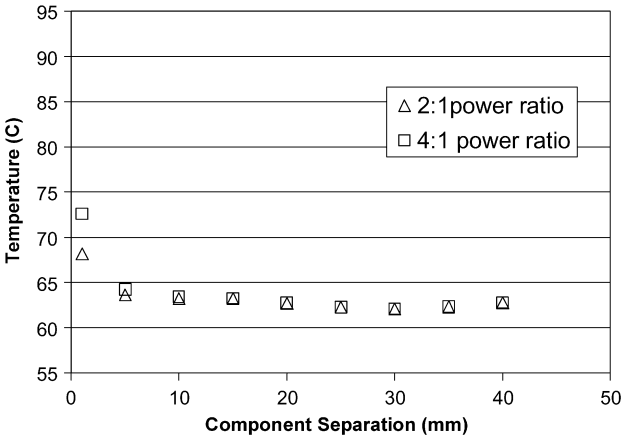


Fig. 6. Device operating temperature as a function of device power ratio for a single FR-4 board, long rectangle device.

4.1. Device operating temperature and plateau distance

Fig. 3 also shows the effect of device geometry on the operating temperature. All devices occupy the same total footprint (12.85 ± 0.04 cm^2), but take different aspect ratios. It can be seen in Fig. 3 that the square and tall rectangle devices attain very similar plateau temperatures, while the plateau temperature for the long rectangle devices is 8.7% lower for the low power device and 10% lower for the high power device. This reduction in operating temperature is beneficial to the device and is related to the development of the natural convection boundary layer over the different device geometries and the interaction of natural convection and board conduction for the differently shaped conduction footprints.

While a strong effect of device geometry is seen on device operating temperature, there is only a weak effect seen on the plateau distance. Plateau distance is defined as the separation distance at which the plateau temperature is achieved and the neighboring devices no longer thermally influence each other. For all six conditions depicted on Fig. 3, the plateau distance occurs between 5 and 10 mm.

The effect of circuit board fabrication on device operating temperature and plateau distance is shown in Fig. 5. As expected, the conductivity of the base circuit board has a significant effect on the device operating temperature. Fig. 5 shows the effects of board conductivity on the operating temperature of a long rectangle, low power device operating with a 2 : 1 power ratio. The copper cladding, which simulates a heavily populated board with many electrical traces, reduces the overall operating temperature of the device as more heat is dissipated through board conduction (along the traces) rather than by natural convection. A reduction in plateau temperature of 26% (62.5 °C to 45.8 °C) and a reduction in peak temperature of 24% (68.17 °C to 51.82 °C) are seen between the FR4 board and the copper clad board. Fig. 5 also illustrates a longer plateau distance for the copper clad board, which results from the greater board conductivity creating a larger thermal footprint. It is when the devices are located within the thermal footprint of its neighbor that neighbor heating effects are highest, so the larger thermal footprint leads to a greater plateau distance. On the copper clad board, the devices must be spaced 20 mm apart to eliminate any neighbor heating effects, compared to 5–10 mm for the FR4 board. Locating the devices closer than this 20 mm plateau distance can lead to significant increases in operating temperature, as seen for the FR4 board. For the copper clad board in this case, the operating temperature increases as much as 6 °C, a 13% increase (from 45.8 °C to 51.8 °C peak).

The effect of device power ratio on plateau distance and operating power can be seen in Fig. 6. Fig. 6 depicts the operating temperature of the lower power device on a single FR4 board with long rectangle devices. In both cases, the low power device dissipates 2.5 W, but in the 2 : 1 power ratio case it is mounted in close proximity to a 5 W device and in the 4 : 1 power ratio case it is mounted in close proximity to a 10 W device. Interestingly, in the plateau region, the effect of this power ratio is found to be insignificant as the devices are not thermally influencing each other, and the devices reach the same plateau temperature. However, as the device spacing declines, the device located in close proximity to the 10 W device reaches an operating temperature 6.5% higher than the identical device in close proximity to the 5 W device. Additionally, the plateau distance is extended for the higher power ratio case, again due to the larger thermal footprint for the higher power device. The operating temperature of the higher power device is strongly affected by the power ratio because the power it is dissipating increases from 5 to 7.5 to 10 W as power ratio increases from 2 : 1 to 4 : 1.

The influence of circuit board spacing on the device temperature is seen in Fig. 7. Fig. 7 depicts the operating temperature of the lower power device on each of two identical FR4 boards. The devices all have the long rectangle geometry, operate at 2.5 W and are in near proximity to an identical device operating at 5 W. A strong influence of board spacing is seen on device operating temperature. As the boards move closer together, the device operating temperature increases once a threshold distance is passed. It is seen that the device operating temperatures are similar for the 25 mm and 40 mm board spacing, but significantly higher for the 10 mm spacing. For the 25 mm and 40 mm casing, the channel width is large enough that the individual boards function as isolated plates while for the 10 mm

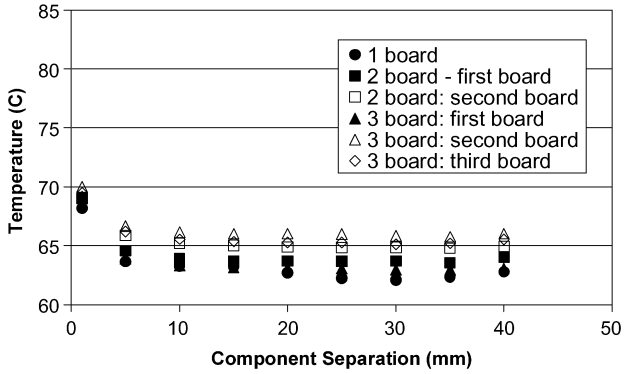


Fig. 7. Device operating temperature as a function of the number of identical circuit boards for the lower power long rectangle device operating with a 2 : 1 power ratio on multiple identical FR4 boards with 10 mm spacing between boards.

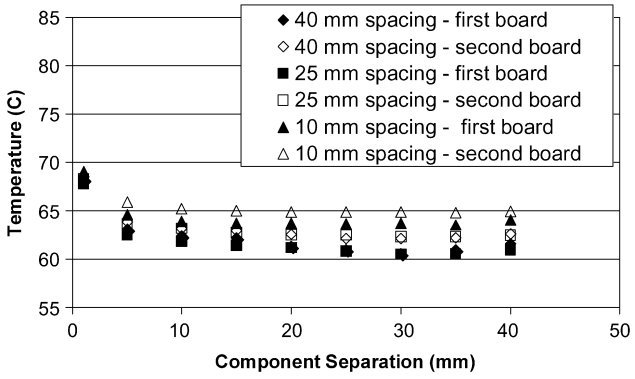


Fig. 8. Device operating temperature as a function of the circuit board spacing for the low power long rectangle device operating with a 2 : 1 power ratio on two identical FR4 boards.

spacing, significant channel effects occur, increasing the device operating temperature.

The effect of circuit board packing is shown in Fig. 8. Fig. 8 depicts the operating temperature of the lower power device(s) when located on one, two or three identical FR4 boards with 10 mm spacing between boards. The devices all have the long rectangle geometry, operate at 2.5 W and are in near proximity to an identical device operating at 5 W. Although all devices operate at 2.5 W, the devices located in multiple board sets reach higher operating temperatures. The lowest device temperatures occur on the single board and the highest device operating temperatures occur on the middle board of the three board set.

These effects can be explained by the heating influence of the additional boards. A single board operates thermally without any influence from neighbors, as additional identically populated boards are added, asymmetrically heated channels are formed which funnel the air flow over the devices. The heat dissipation from the devices on the additional boards warms the air in the channel, which flows across the rear of the first board as well as across the devices on the 2nd board. In all cases, the devices on the first board have the coolest operating temperatures, but increase as additional boards are added. The highest device operating temperatures occur on the 2nd board of the 3rd board

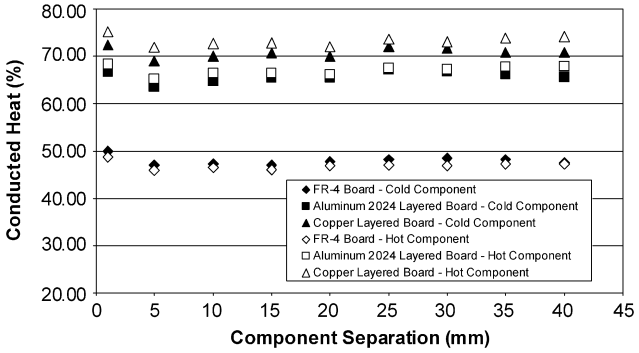


Fig. 9. The effect of board conductivity on percentage of heat conducted for a 2 : 1 power ratio, long rectangle device geometry on a single board.

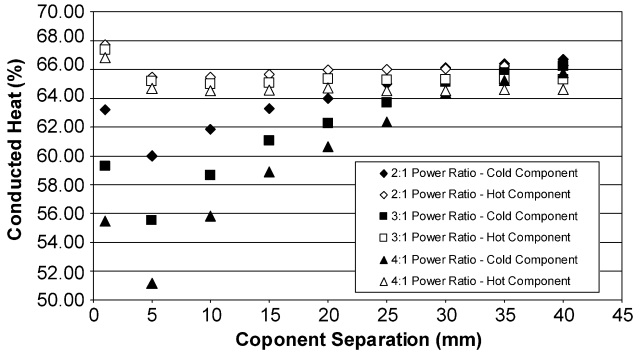


Fig. 10. The effect of power ratio on percentage of heat conducted for square device geometry.

configuration because the 2nd board experiences its own heat dissipation as well as warming effects from both the first and third boards.

Despite this strong influence on device operating temperature, little influence of the number of boards is seen on plateau distance. In all cases the plateau distance is about 10 mm and the plateau temperature remains relatively constant after that point.

4.2. Device power dissipation

The model results show that conduction into the printed circuit board is the primary mode of heat dissipation. The PCB conductivity exhibits the strongest influence on the percentage of heat dissipated by board conduction. As expected, as the conductivity of the board increases, the amount of power dissipated by conduction also increases (Fig. 9). For a sparsely populated board, represented by the plain FR4 board approximately 45% of the waste heat is dissipated by conduction into the board with the rest dissipated by radiation and natural convection, while for a densely populated board, represented by the copper clad board, the percentage of waste heat dissipated by conduction exceeds 70%.

Fig. 10 shows that the conduction percentages of the higher power devices are only slightly affected by the change in power ratio while the lower power devices are strongly affected by rising power ratios. The lower power devices exhibit a significant reduction in conduction percentage when device separation dis-

tance is less than 25 mm. This is related to the strong neighbor heating effects seen in this situation. As the higher power device increases its power dissipation, its thermal footprint becomes larger, raising the temperature of the PCB. As the PCB temperature increases, the potential driving force for conduction from the lower power device decreases and conduction is reduced. As separation distance between the devices increases beyond 25 mm, the neighboring effects between the higher power and lower power devices decline and the percentage of heat dissipated by conduction for the lower power device increases to approximately the same conduction percentage as the higher power devices.

There is virtually no effect on the percentage of heat conducted with a change in device geometry as the contact area of the device is the same for all device designs. The effect of the number of identical boards and board separation distance on the percentage of waste heat dissipated by conduction is found to be small.

4.3. Design of experiments data regression

The parametric study is designed using Design of Experiments (DOE) methodology to interpret the interaction between parameters. For this analysis, the five parameters (board packing density, board conductivity, device geometry, power density, and board separation distance) were organized into a matrix of 27 different analysis cases using a five factor face-centered central composite DOE (FCCCD) model to explore parameter interactions. The DOE software used for this analysis was DOE KISS which works within Excel. DOE KISS allow the creation and analysis of DOE matrices using multiple regression modeling.

The DOE matrix was analyzed using the steady-state plateau region device operating temperatures resulting from each of the computational trials. For a general DOE analysis, the data regression yields an equation for the dependent parameter as a function of each independent parameter and includes interactions between parameters. In this case, the matrix is analyzed to solve for the coefficients to get an equation for device operating temperature as a function of each parameter and combination of parameters.

The matrix can be analyzed using the -1, 0 and 1 for each parameter in the matrix or the actual parameter value. The only benefit to use the -1, 0, 1 value is to indicate the relative influence of each parameter on device operating temperature. The larger the multiplying coefficient is, the larger the effect of the independent parameter. A negative coefficient represents an inverse relationship with the parameters. Table 1 lists the physical parameters denoted by variables A through E. Eq. (3) shows the result from the multiple regression using the -1, 0, 1 value to indicate the relative influence of each parameter on the higher power device operating temperature and illustrates that board conductivity and power ratio have the largest influence. In contrast, as seen in Eq. (4) for the lower power device the board conductivity is still influential but the power ratio is not. Power ratio plays no role in lower power device operating temperature because this equation considers on the plateau region temperature where the neighbor influence of the high power device has subsided and the lower power device power dissipation remains constant at 2.5 W.

Table 1
DOE variables in equations from statistical regression

DOE variable	Actual parameter	Units
A	Board packing density	
B	Board conductivity	$\mathrm{W\,m^{-1}\,K^{-1}}$
C	Component geometry	height [mm]
D	Power density	W
E	Multiple board separation distance	mm

$$\begin{aligned}\textit{Weighted Temp}_{\text{high power device}} &= 0.93525 \cdot A - 22.674 \cdot B + 5.71923 \cdot C + 21.090 \cdot D \\ &\quad - 1.19620 \cdot E \end{aligned} \tag{3}$$

$$\begin{aligned}\textit{Weighted Temp}_{\text{low power device}} &= 1.35228 \cdot A - 7.60358 \cdot B + 3.42590 \cdot C + 0.99525 \cdot D \\ &\quad - 1.25201 \cdot E \end{aligned} \tag{4}$$

In these equations, parameters and combinations of parameters with coefficients at least two orders of magnitude smaller than the others and thus of negligible influence are dropped for simplicity.

The DOE matrices were analyzed a second time using the actual values for each parameter in place of the -1, 0 and 1 values to find a detailed equation for predicting the device operating temperature with respect to these parameters. These equations (Eqs. (5) and (6)) allow the calculation of predicted device operating temperature in the plateau region. The R^2 value for Eq. (5) is 0.9996 and for Eq. (6) is 0.9983. The results of these equations match the device temperatures predicted by IcePak within 5–10%. It should be noted that these equations are strictly valid only for the situation analyzed in this case, but may serve as a rule of thumb or simple predictive method for the thermal designer.

$$\begin{aligned}\textit{Temperature}_{\text{hot}} &= 10.703 + 2.37223 \cdot A - 0.12334 \cdot B + 1535.7 \cdot C \\ &\quad + 30.563 \cdot D - 253.334 \cdot E + 0.00431 \cdot A \cdot B \\ &\quad + 17.997 \cdot A \cdot C + 0.06382 \cdot A \cdot D - 90.069 \cdot A \cdot E \\ &\quad - 0.47772 \cdot B \cdot C - 0.02870 \cdot B \cdot D - 0.10862 \cdot B \cdot E \\ &\quad + 51.207 \cdot C \cdot D + 130.612 \cdot C \cdot E - 15.625 \cdot D \cdot E \\ &\quad - 0.22125 \cdot A^2 + 0.000267416 \cdot B^2 - 18342.4 \cdot C^2 \\ &\quad - 0.88208 \cdot D^2 + 8353.7 \cdot E^2 \end{aligned} \tag{5}$$

$$\begin{aligned}\textit{Temperature}_{\text{cold}} &= 50.192 + 2.90894 \cdot A - 0.08998 \cdot B \\ &\quad + 682.617 \cdot C + 1.22414 \cdot D - 271.471 \cdot E \\ &\quad + 0.00203 \cdot A \cdot B + 20.453 \cdot A \cdot C + 0.21819 \cdot A \cdot D \\ &\quad - 57.407 \cdot A \cdot E - 0.11485 \cdot B \cdot C + 0.00317 \cdot B \cdot D \end{aligned}$$

$$- 0.02390 \cdot B \cdot E + 13.749 \cdot C \cdot D - 391.579 \cdot C \cdot E - 14.093 \cdot D \cdot E - 0.47882 \cdot A^2 + 0.000107485 \cdot B^2 - 7550.0 \cdot C^2 - 0.23993 \cdot D^2 + 7278.1 \cdot E^2 \quad (6)$$

5. Conclusions

Neighbor effects have been studied for two unequally heated devices on tall circuit boards dissipating heat by natural convection, radiation and board conduction. The results show that when two powered devices are within a certain threshold spacing, referred to here as plateau spacing, the higher power device thermally influences the lower power device by increasing the operating temperature of the lower power device. At device spacings exceeding the plateau spacing, each device reaches an operating temperature that is independent of spacing. The influence of various parameters including device geometry, circuit board fabrication, power ratio between devices, number of boards and spacing between boards on plateau distance and on device operating temperature have been quantified. The strongest effects on plateau distance were caused by power ratio between the two devices and the circuit board conductivity. Number of boards, board spacing and device geometry were found to have little effect on plateau distance. However, all five parameters were found to have a significant effect on device operating temperature. The device operating temperature was found to increase with power ratio and the number of identical circuit boards in the enclosure. The device operating temperature was found to vary inversely with device spacing and circuit board conductivity.

These parameters were analyzed using trials determined by a face-centered central composite DOE (FCCCD) model and the results have been reduced with data regression to develop predictive equations for device operating temperature which illustrate the relative influence of each studied parameter. The methods developed here will allow designers to quickly explore design parameters and identify those with the most influence on thermal interactions so that these interactions can be minimized or eliminated in the final product.

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